

CLAIMS

What is claimed is:

5 1. A method for forming a MOSFET, said method comprises:

 providing a wafer, wherein said wafer comprises a substrate;

 forming a trench in said substrate;

 forming a gate on a bottom of said trench;

10 forming a spacer on both sides of said gate and filling of said trench;

 implanting a ion into said substrate which is on both sides of said spacer;

 proceeding a first rapid thermal process to form a source/drain region and a source/drain extended region in said substrate;

15 forming a metal layer on said gate, said spacer, and said source /drain region;

 proceeding a second rapid thermal process to form a silicide layer on said gate and said source/drain region; and

20 removing said metal layer.

 2. The method according to claim 1, wherein said gate comprises a gate oxide layer.

25 3. The method according to claim 1, wherein a depth of said trench is 50% to 80% of a thickness of said gate.

 4. The method according to claim 1, wherein said ion is a

N type ion.

5. The method according to claim 1, wherein said ion is a P type ion.

6. The method according to claim 1, wherein said a material of said metal layer is titanium.

7. The method according to claim 1, wherein said a material of said metal layer is cobalt.

8. The method according to claim 1, wherein said a material of said metal layer is platinum.

9. A method for forming a MOSFET, said method comprises:

providing a wafer, wherein said wafer comprises a substrate;

forming a trench in said substrate;

forming a gate on a bottom of said trench, wherein said gate comprises a gate oxide layer;

forming a spacer on a sidewall of said gate and said gate oxide layer and filling of said trench;

implanting a ion into said substrate which is on both sides of said spacer;

proceeding a first rapid thermal process to form a source/drain region and a source/drain extended region in said substrate;

forming a metal layer on said gate, said spacer, and said source /drain region;

proceeding a second rapid thermal process to form a silicide layer on said gate and said source/drain region; and removing said metal layer and proceeding a third rapid thermal process.

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10. The method according to claim 9, wherein a depth of said trench is 50% to 80% of a thickness of said gate.

10 11. The method according to claim 9, wherein said ion is a N type ion.

12. The method according to claim 9, wherein said ion is a P type ion.

15 13. The method according to claim 9, wherein said a material of said metal layer is titanium.

20 14. The method according to claim 9, wherein said a material of said metal layer is cobalt.

15. The method according to claim 9, wherein said a material of said metal layer is platinum.

25 16. The method according to claim 9, wherein a material of said spacer is silicon nitride.

17. The method according to claim 9, wherein a temperature of said first rapid thermal process is about 950°C to 1050

Figure 1. Schematic representation of the experimental design. The subjects were divided into two groups: the control group (CG) and the experimental group (EG). The CG was divided into two subgroups: the control group (CG) and the control group (CG). The EG was divided into two subgroups: the experimental group (EG) and the experimental group (EG). The subjects were divided into two groups: the control group (CG) and the experimental group (EG). The CG was divided into two subgroups: the control group (CG) and the control group (CG). The EG was divided into two subgroups: the experimental group (EG) and the experimental group (EG).

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